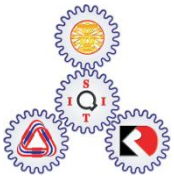


Sirindhorn International Institute of Technology

Thammasat University at Rangsit

School of Information, Computer and Communication Technology

ECS 371: Problem Set 10 Solution

Semester/Year: **1/2009**
Course Title: Digital Circuits
Instructor: Dr. Prapun Suksompong (prapun@siit.tu.ac.th)
Course Web Site: http://www.siit.tu.ac.th/prapun/ecs371/

Due date: September 23, 2009 (Wednesday)

Instructions

1. Only ONE of the problems will be graded. Of course, you do not know which problems will be selected; so you should work on all of them.
2. Late submission will not be accepted.
3. ***Write down all the steps*** that you have done to obtain your answers. You may not get full credit even when your answer is correct without showing how you get your answer.

Chapter 9:

1. Why are shift registers considered basic memory devices?

Solution: Shift registers ***store*** binary data in a series of flip-flops or other storage elements.

2. What is the storage capacity of a register that can retain two bytes of data?

Solution: 1 byte = 8 bits; 2 bytes = **16 bits**

3. Name two functions of a shift register.

Solution: Shift data and store data

4. The sequence 1011 is applied to the input of a 4-bit serial shift register that is initially cleared. What is the state of the shift register after three clock pulses?

Solution:

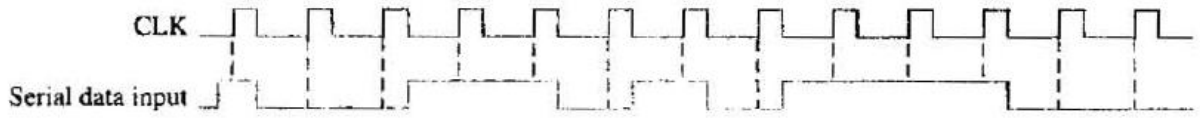
Initially: 0000

After 1st CLK: 1000

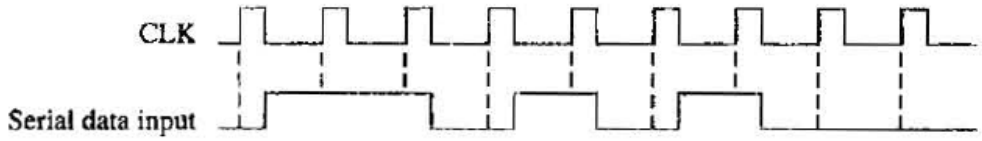
After 2nd CLK: 1100

After 3rd CLK: 0110

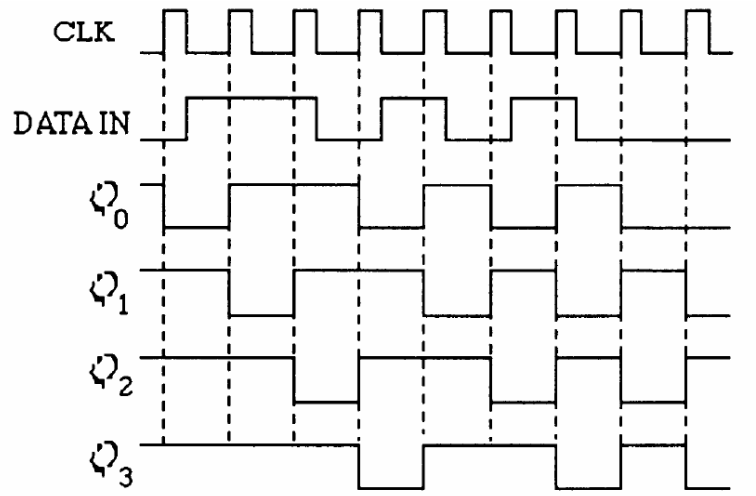
5. For the data input and clock in Figure 9–48, determine the states of each flip-flop in the shift register of Figure 9–3 and show the Q waveforms. Assume that the register contains all 1s initially.



6. Solve Problem 5 for the waveforms in Figure 9–49.

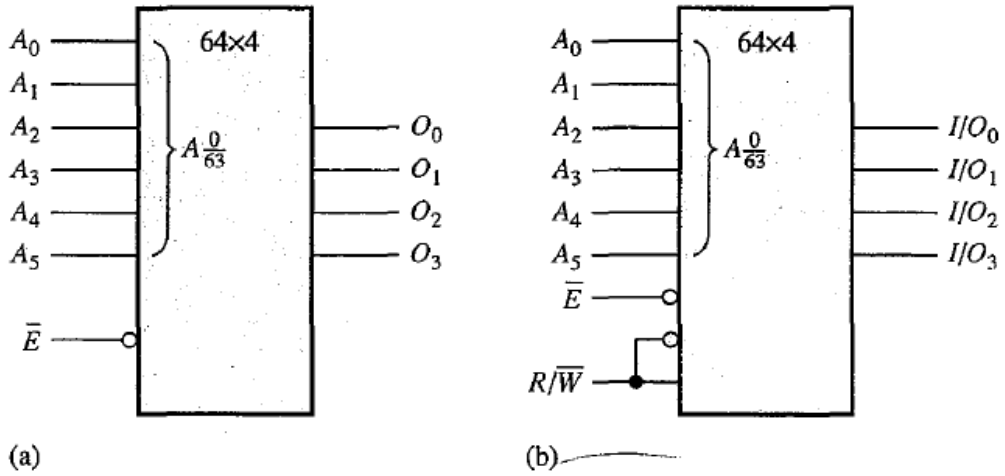


Solution:



Chapter 10:

1. Identify the ROM and the RAM in Figure 10–75.



Solution:

(a) ROM: no read/write control
(b) RAM

2. Explain why RAMs and ROMs are both random-access memories.

Solution:

They are random access memories because any address can be accessed at any time. You do not have to go through all the preceding addresses to get to a specific address.

3. Explain the purposes of the address bus and the data bus.

Solution:

Address bus provides for transfer of address code to memory for accessing any memory location in any order for a read or a write operation.

Data bus provides for transfer of data between the microprocessor and memory or input/output devices.

9. Explain the difference between a SRAM and a DRAM.

Solution: The difference between SRAM and DRAM is that data in a SRAM are stored in latches or flip-flops indefinitely as long as power is applied while data in a DRAM are stored in capacitors which require periodic refreshing to retain the stored data.

10. What is the capacity of a DRAM that has twelve address lines?

Solution: The bit capacity of a DRAM with 12 address lines is $2^{2 \times 12} = 2^{24} = 16{,}777{,}216$ bits = **16 Mbits**

12. Determine the truth table for the ROM in Figure 10–77.

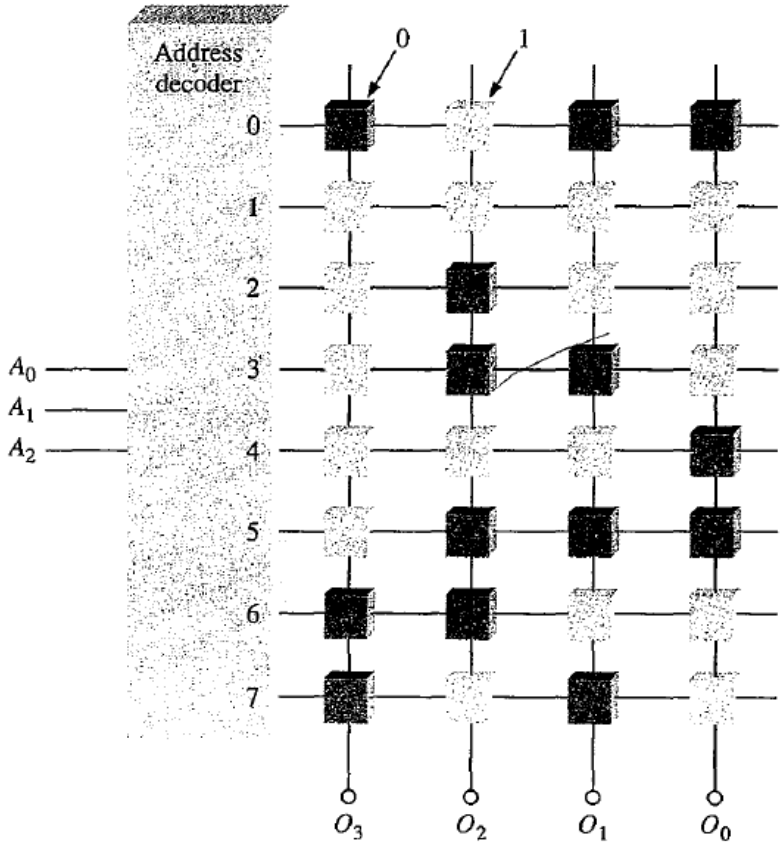


FIGURE 10–77

Solution:

Inputs			Outputs			
A_2	A_1	A_0	O_3	O_2	O_1	O_0
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	1	0	0	1
1	0	0	1	1	1	0
1	0	1	1	0	0	0
1	1	0	0	0	1	1
1	1	1	0	1	0	1